

**FEATURES**

- Double Side Cooling
- High Surge Capability

**APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

**VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR1610F28	2800	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 100\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR1610F26	2600	
DCR1610F24	2400	

Lower voltage grades available.

**ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

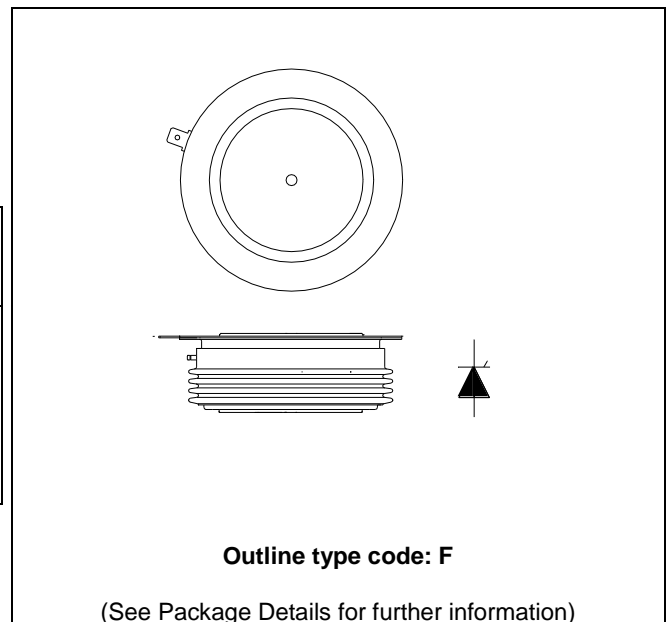
**DCR1610F28**

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

**KEY PARAMETERS**

$V_{DRM}$	<b>2800V</b>
$I_{T(AV)}$	<b>1610A</b>
$I_{TSM}$	<b>21500A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$di/dt$	<b>1000A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available



**Fig. 1 Package outline**

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1607	A
$I_{T(RMS)}$	RMS value	-	2524	A
$I_T$	Continuous (direct) on-state current	-	2353	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	21.5	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	2.3	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

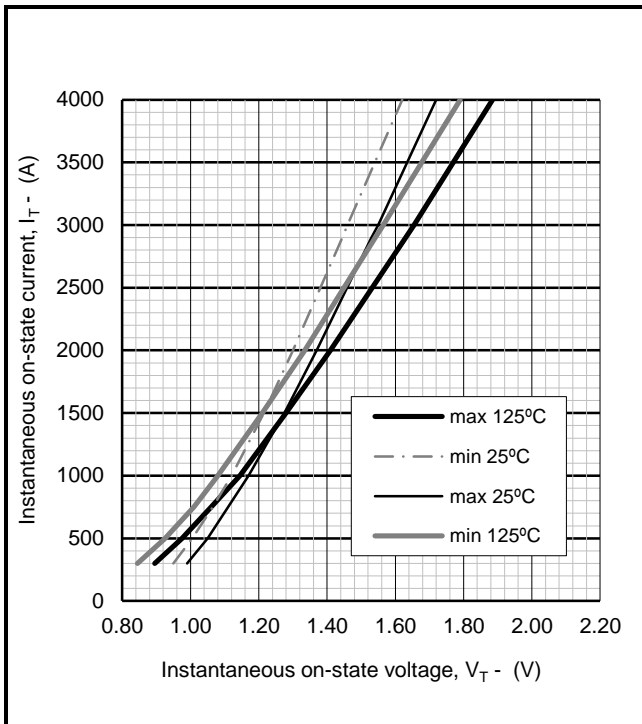
Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0184	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0333	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0418	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23kN (with mounting compound)	Double side	-	0.004	$^{\circ}\text{C/W}$
			Single side	-	0.008	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		22.0	25.0	kN	

**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	100	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$dI/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	250	A/ $\mu s$
		Gate source 30V, $10\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	1000	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	100A to 1000A at $T_{case} = 125^{\circ}C$	-	0.8	V	
	Threshold voltage – High level	1000A to 4000A at $T_{case} = 125^{\circ}C$	-	0.91	V	
$r_T$	On-state slope resistance – Low level	100A to 1000A at $T_{case} = 125^{\circ}C$	-	0.35	$m\Omega$	
	On-state slope resistance – High level	1000A to 4000A at $T_{case} = 125^{\circ}C$	-	0.245	$m\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, $10\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 100V$ , $dI/dt = 5A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear to 2500V	-	600	$\mu s$	
$Q_S$	Stored charge	$I_T = 1000A$ , $t_p = 1000\mu s$ , $T_j = 125^{\circ}C$ , $dI/dt = 5A/\mu s$ ,	2500	3500	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

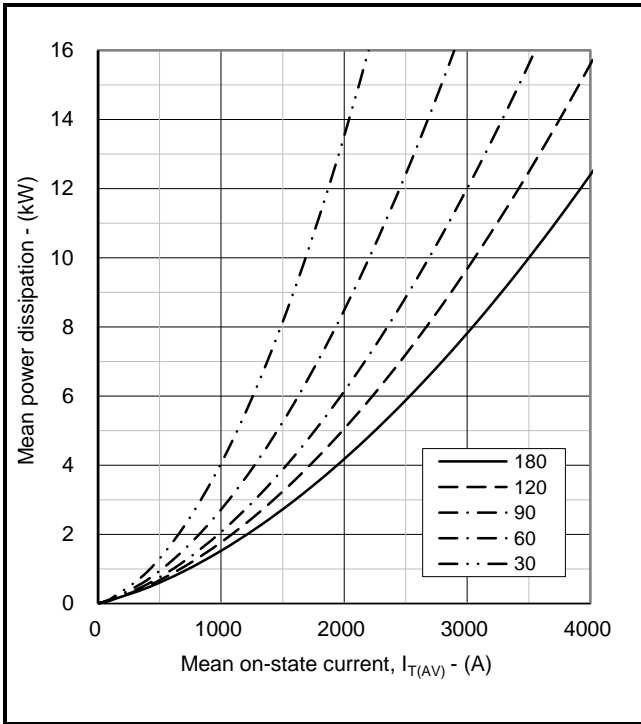
Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	250	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

**CURVES**

**Fig.2 Maximum & minimum on-state characteristics**
**V<sub>TM</sub> EQUATION**

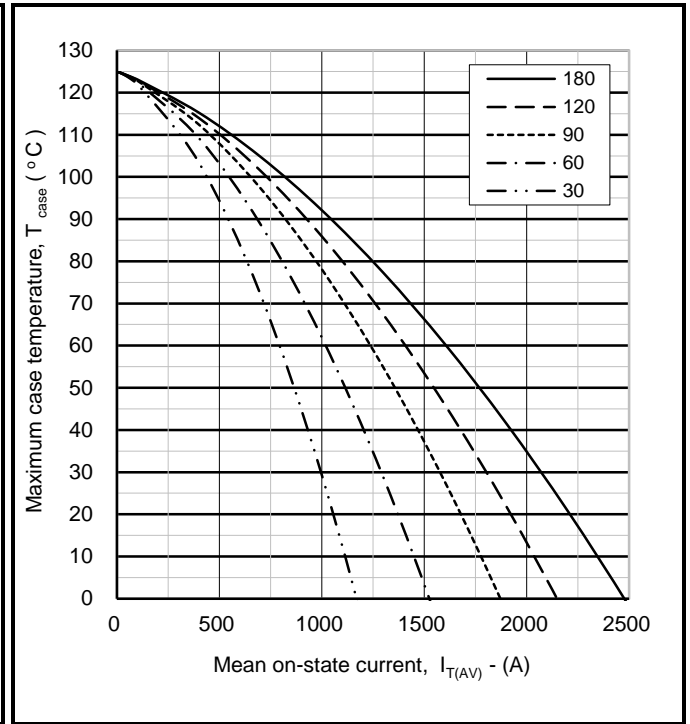
$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.746516  
 B = -0.012797  
 C = 0.000146  
 D = 0.010555

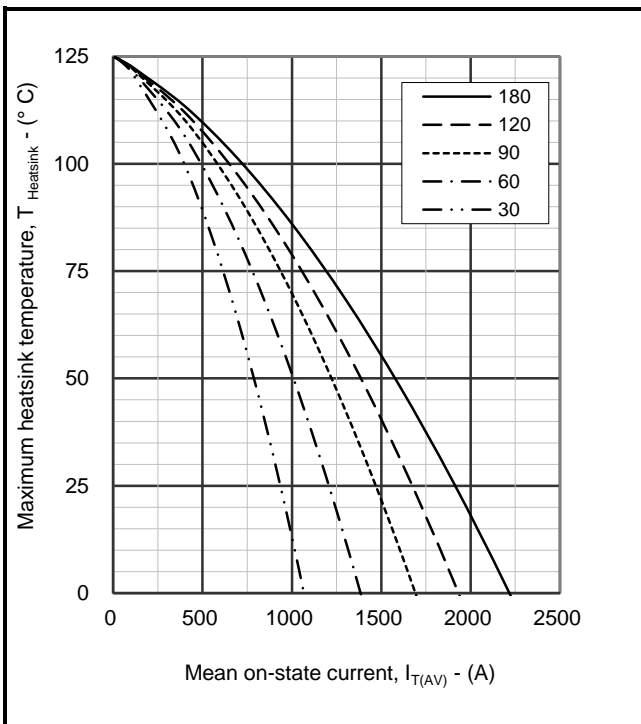
these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 100A to 4000A



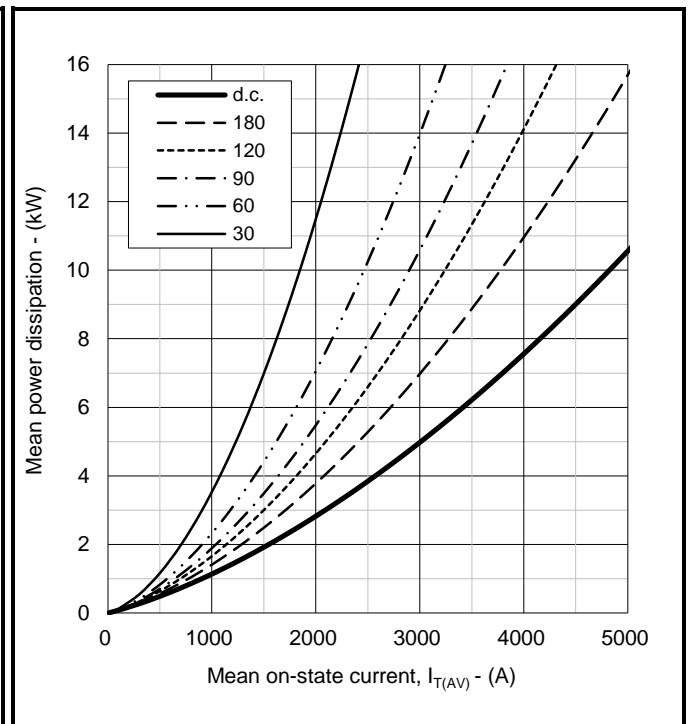
**Fig.3 On-state power dissipation – sine wave**



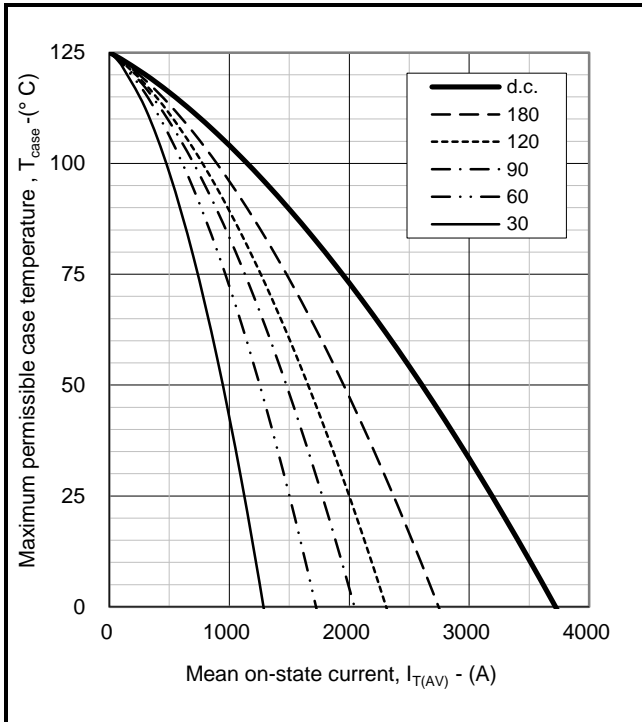
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



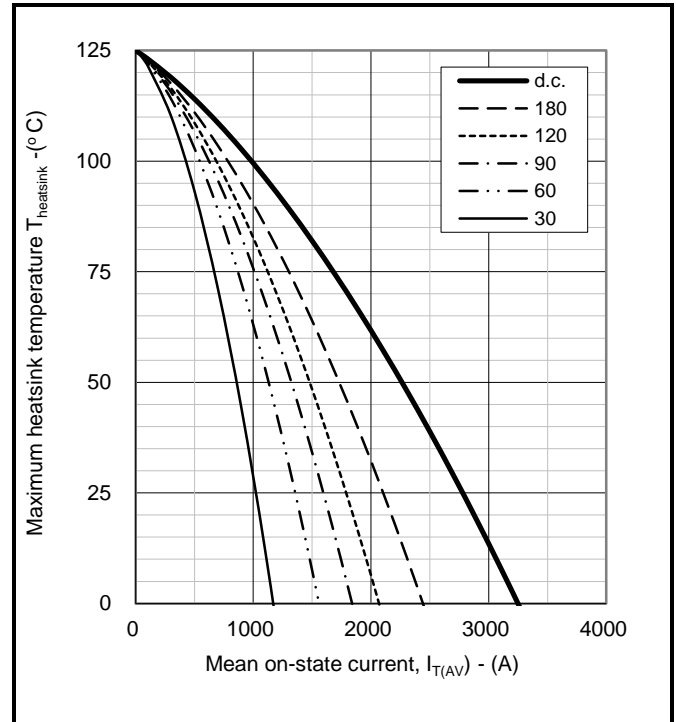
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



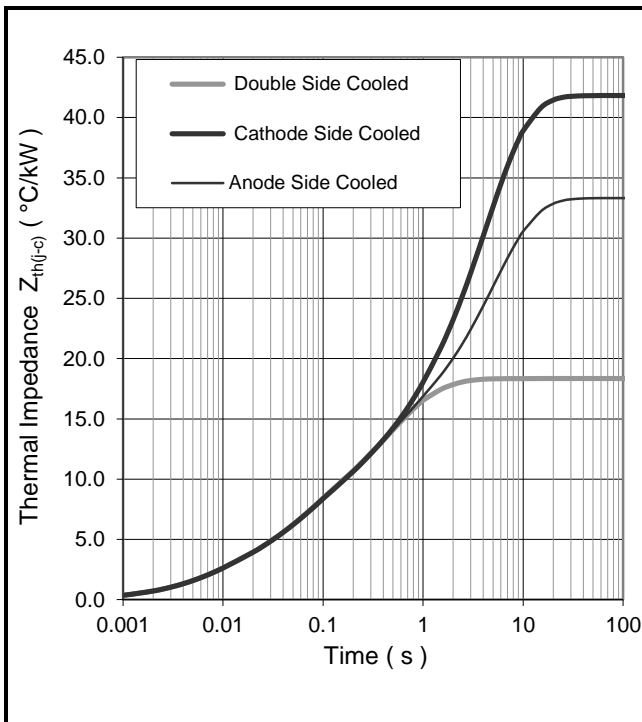
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	7.5608	4.0772	3.8420	2.8671
	T <sub>i</sub> (s)	0.6877	0.2537	0.0614	0.0101
Anode side cooled	R <sub>i</sub> (°C/kW)	6.7211	4.6219	15.5387	14.8631
	T <sub>i</sub> (s)	0.1910	0.0158	5.0011	3.3169
Cathode side cooled	R <sub>i</sub> (°C/kW)	11.5564	8.5810	4.7942	8.3643
	T <sub>i</sub> (s)	4.2216	6.0269	0.0166	0.2255

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(-T / T_i))]$$

**ΔR<sub>th(j-c)</sub> Conduction**

Tables show the increments of thermal resistance R<sub>th(j-c)</sub> when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.		sine.	rect.		sine.	rect.
180	3.19	2.14	180	2.97	2.03	180	2.95	2.02
120	3.72	3.10	120	3.43	2.89	120	3.40	2.87
90	4.29	3.64	90	3.92	3.36	90	3.88	3.34
60	4.81	4.23	60	4.36	3.87	60	4.31	3.84
30	5.22	4.88	30	4.69	4.41	30	4.64	4.37
15	5.40	5.22	15	4.84	4.70	15	4.79	4.65

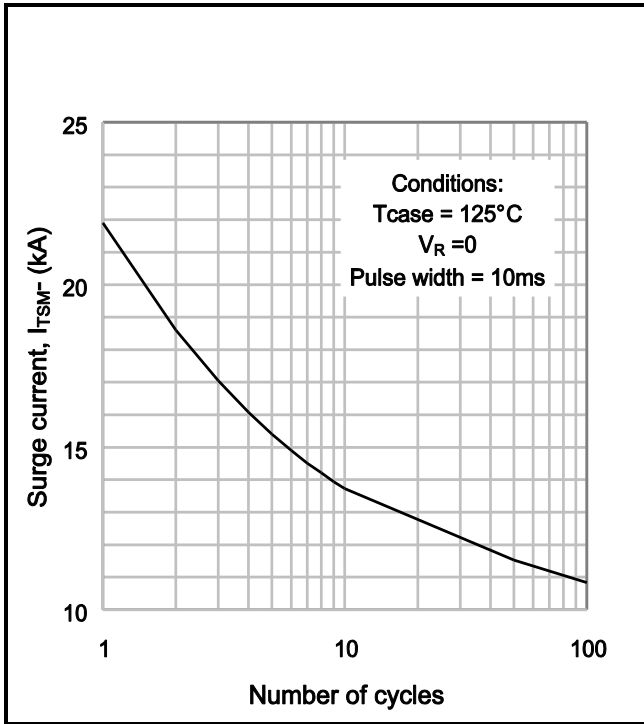


Fig.10 Multi-cycle surge current

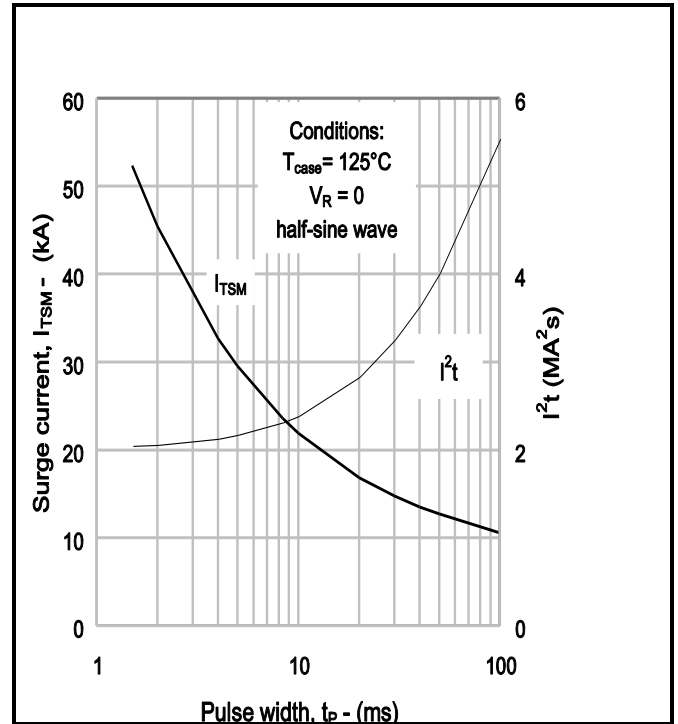


Fig.11 Single-cycle surge current

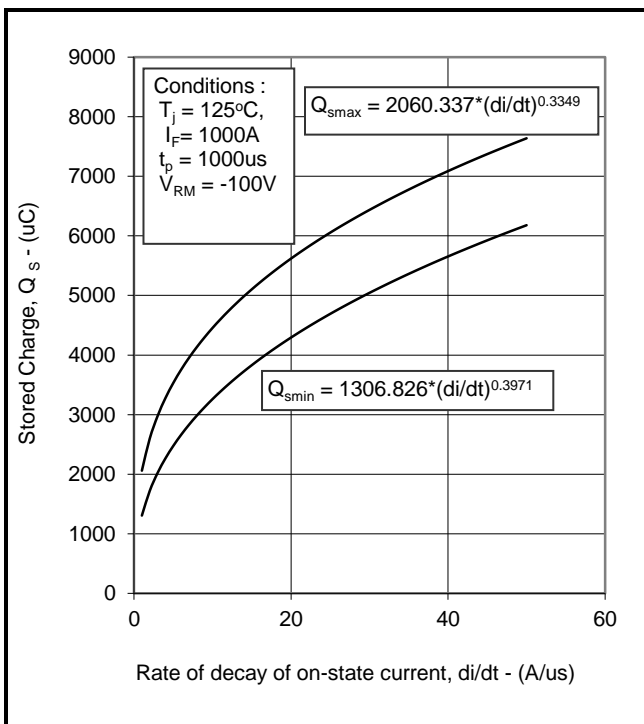


Fig.12 Stored charge vs di/dt

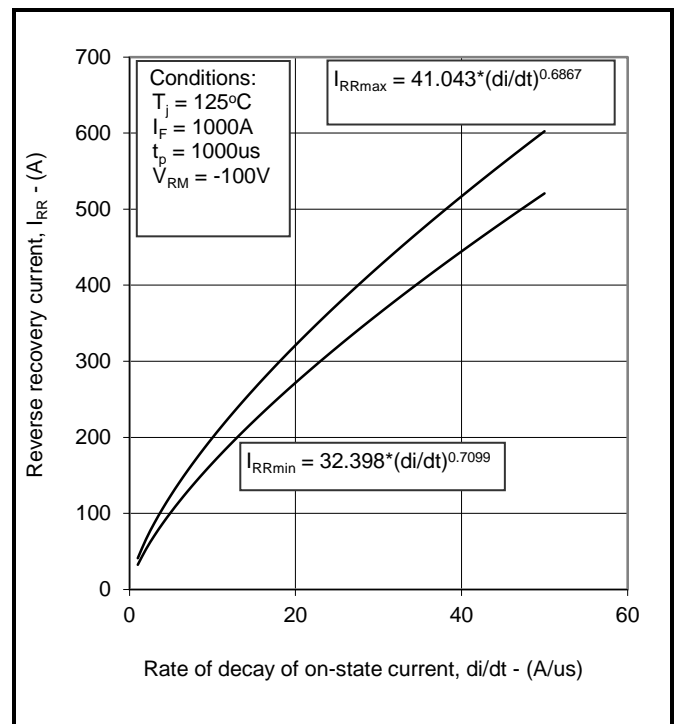
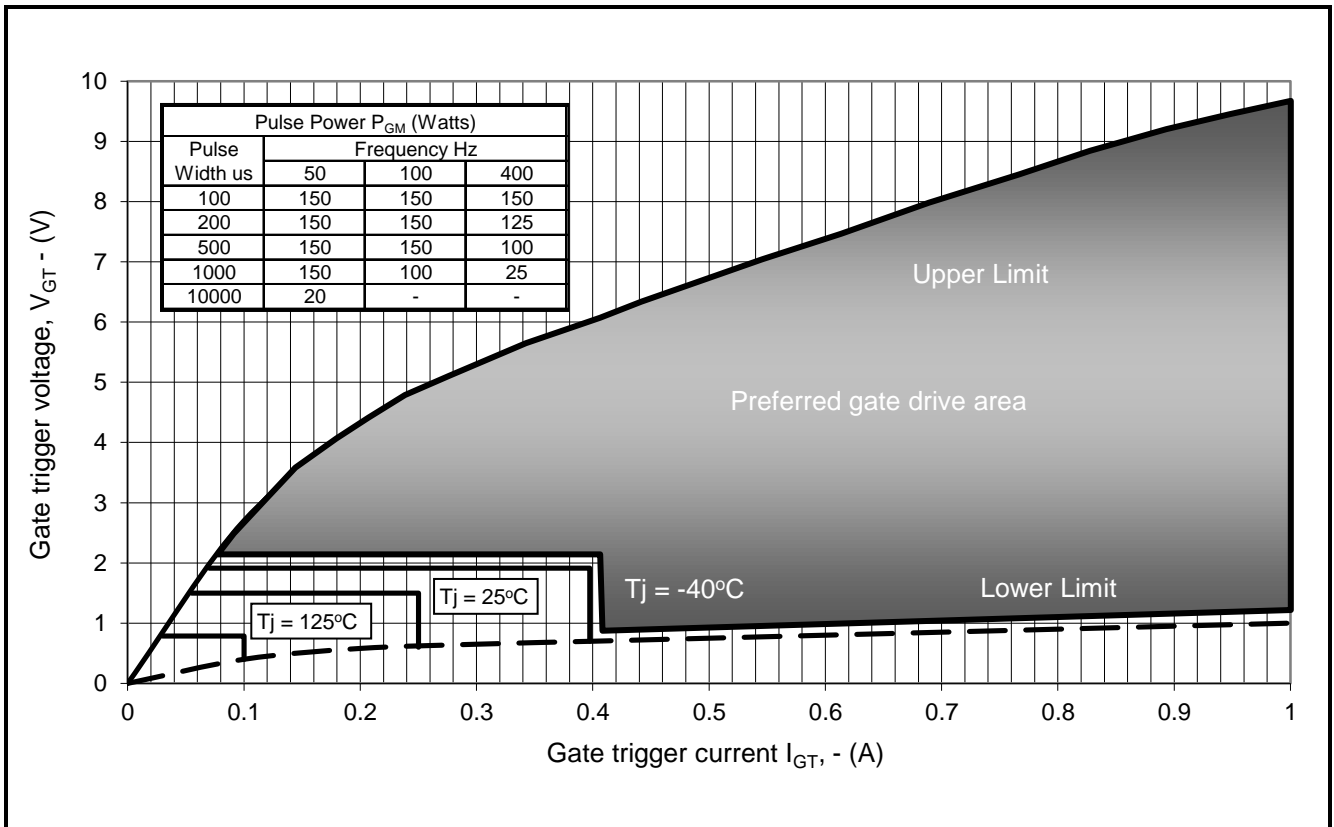
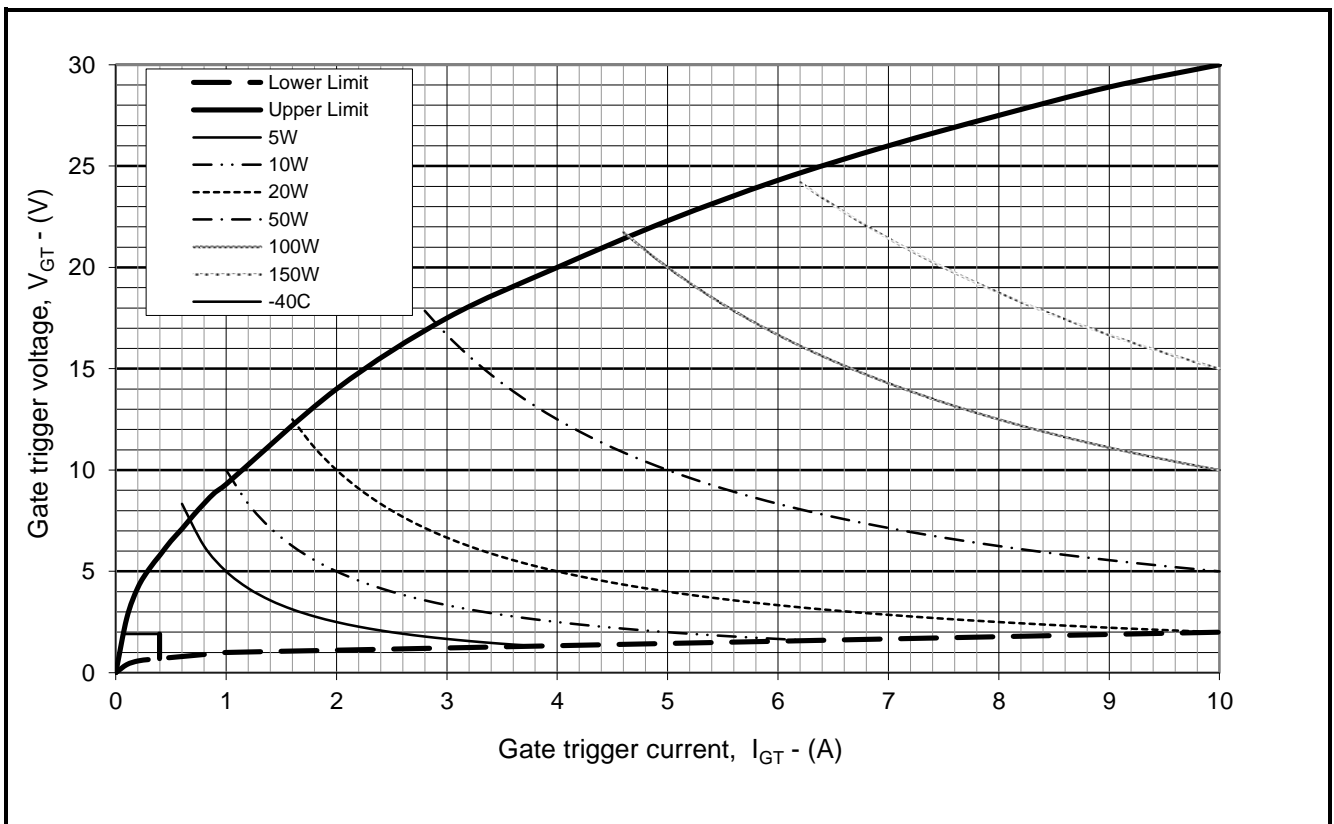


Fig.13 Reverse recovery current vs di/dt



**Fig14 Gate Characteristics**

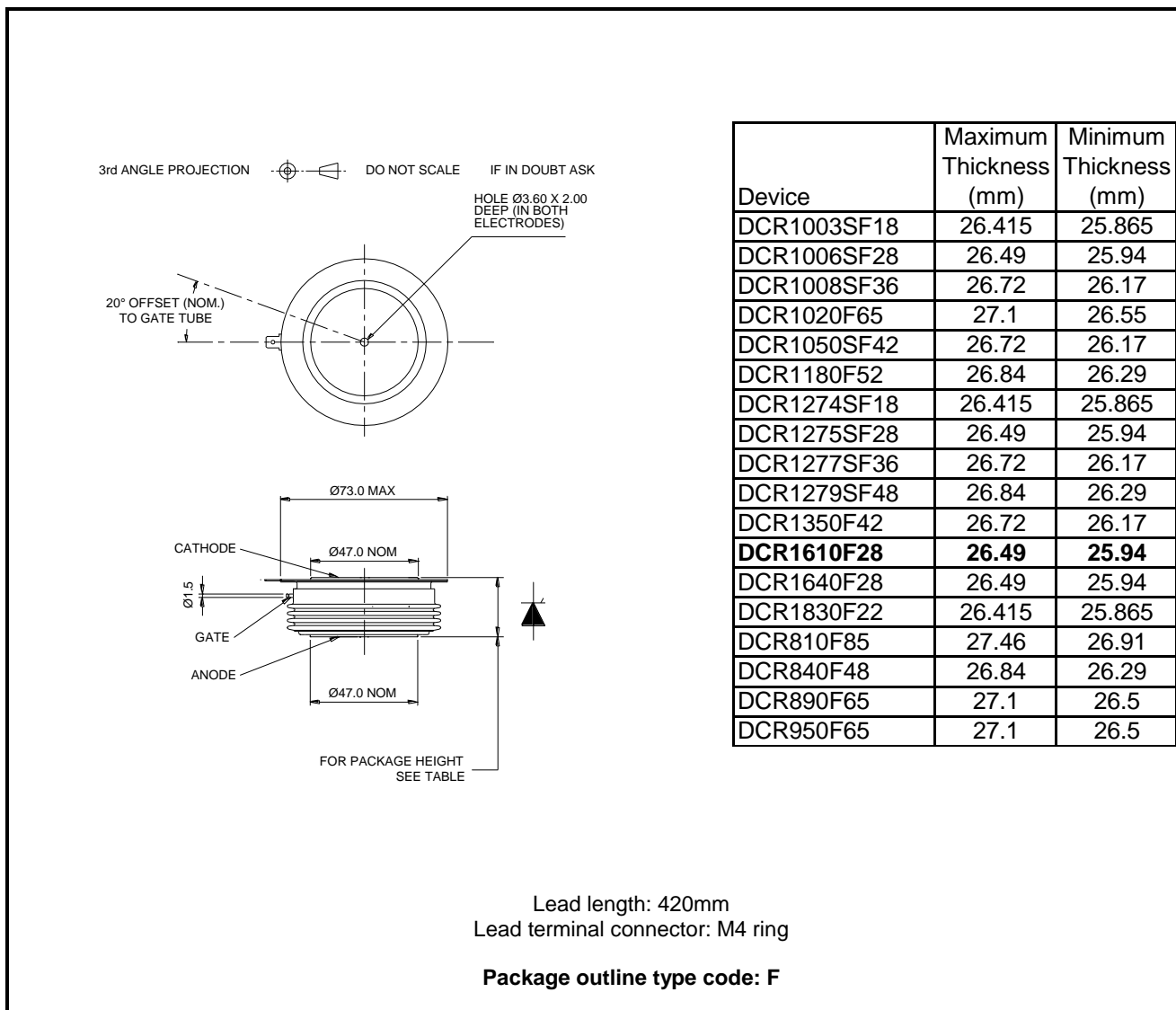


**Fig. 15 Gate characteristics**



**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**


**Fig.16 Package outline**

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

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